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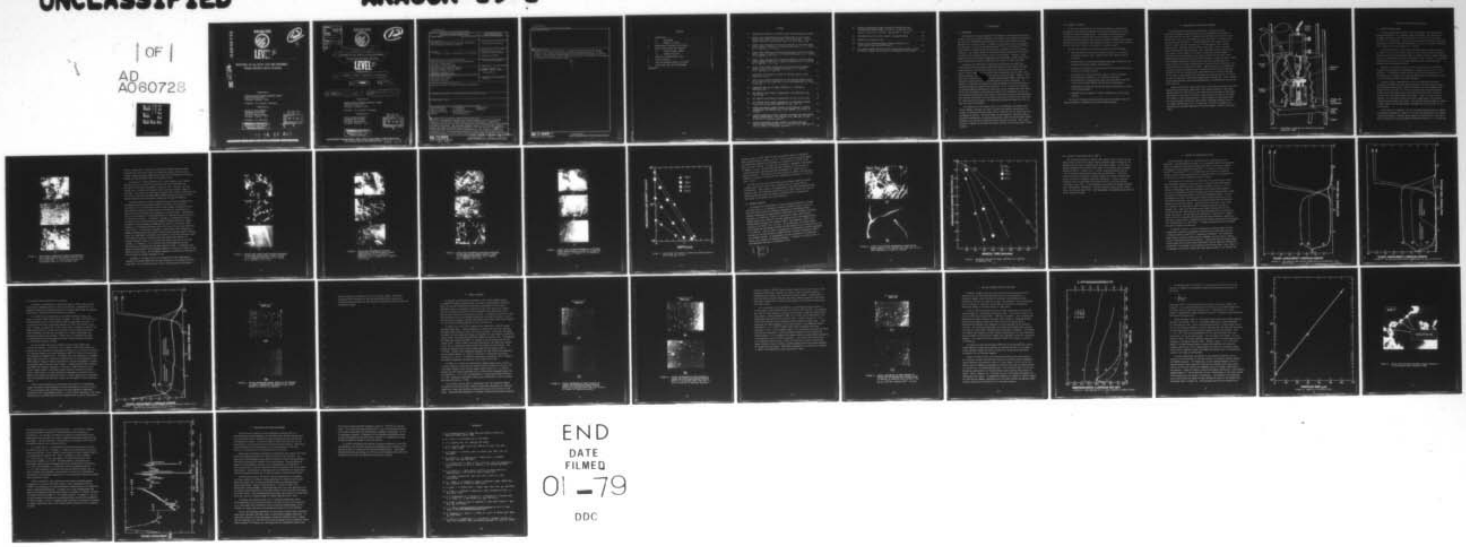

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LEVEL II

IMPROVEMENT IN GaAs DEVICE YIELD AND PERFORMANCE THROUGH SUBSTRATE DEFECT GETTERING

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The use of mechanically produced back-surface-damage as a means of gettering impurities and defects in GaAs wafers has been investigated. Comparative analyses have been done on both ion implantation and mechanical back-surface-damage gettering techniques. The increased thermal stability of mechanically produced damage has shown ion implantation techniques to be less effective for gettering over long anneal periods at elevated temperatures. For anneals at 800° C for periods ≤ 5 hrs, stress gradients produced by graded dislocation distributions produce reductions in front surface defect concentrations and effective gettering

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of Au and Cr at the back surface. For anneal times exceeding the thermal stability time reverse gettering or impurity detrapping occurs at the back surface. Front-surface encapsulating layers have also been shown to exercise a small but perceptible effect related in part to the concentration of As and/or Ga vacancies in the interfacial region.

CONTENTS

FIGURES

1. INTRODUCTION

1.1 BACKGROUND

The influence of surface damage and secondary or included growth defects on the electrical transport properties of elemental and compound semiconductors has been well established and documented in articles and technical reports published over the past decade. A number of investigators have used defects introduced at a surface by mechanical means,[1-4] or by ion implantation[5-8] to control defect or impurity gettering from the opposite surface of the semiconductor. The largest number of studies has been directed toward improving the quality and ultimate device yield of silicon wafers. However, recent applications of back-surface-damage-gettering techniques to GaAs wafers have shown considerable promise for improving the quality of GaAs based FETs.

Studies at the IBM Fishkill Laboratory by Sckwuttke and Yang[1] have demonstrated that back-surface mechanical damaging of GaAs wafers by impact sound stressing can effectively reduce the front surface concentration of defects and the numb[illegible] of dislocation lines propagating from the wafer into active epitaxial laye[illegible] on the surface of the material. However, there have been no detailed stu[illegible] optimize back-surface damage techniques and extend this application to [illegible]al fabrication of device structures. In addition, no detailed information has been published on the effectiveness of controlled damage in impurity gettering GaAs. It is of particular interest to determine whether gettering of impurities such as chromium and other heavy metals can be obtained, since these are known to be responsible in part for the "mobility/concentration dip" effect in epi-layers grown on GaAs substrates. The relative efficiencies of back-surface gettering of defects and impurities by either mechanical damage or ion-implantation-produced damage has also not been previously established.

The objective of the present study is to investigate and compare back-surface damage techniques in regard to defect and impurity gettering in an attempt to optimize procedures that will be effective for the production line processing of devices. The first phase of this program is directed toward a detailed investigation of gettering procedures, while the second phase entails production and testing of prototype device structures on GaAs. This report presents a summary of the first six months activity in the first phase of this program.

1.2 SUMMARY OF RESULTS

In the first six months of the research program, we developed an apparatus for the uniform production of mechanical damage at the back-surfaces of both Si and GaAs wafers. The results of investigations to characterize the distribution and nature of defects introduced by mechanical damage is GaAs, as well as the efficiency of defect and impurity gettering, are summarized in the sections to follow. Detailed descriptions of the results for Si will be included in a separate report.

For the GaAs program, the following results have been obtained:

- o Identification of dislocation line distributions as a function of abrasive particle size, rotation rate, and exposure time of the wafer.
- o Identification of front-surface-defect-gettering efficiencies for variable back-surface-defect concentrations.
- o Consistent evaluation of Cr and Au defect gettering by dislocation structure at the back surface.
- o Investigation of defect stability times or maximum allowable processing times at 800^{o} C. for effective gettering.
- o Identification of encapsulation layer gettering effects and the correlation of these effects with Ga and As outdiffusion.
- o Comparison of mechanical and ion-implantation gettering of defects at the front-surface.
- o Identification of impurity "reverse" annealing or de-gettering effects.

The results obtained in this reporting period and current data are being prepared for presentation in three technical papers.

2. EXPERIMENTAL PROCEDURE AND APPARATUS

The laboratory apparatus for mechanically creating controlled back-surface damage in small samples is shown schematically in Figure 1. The teflon base of the unit is supported by rods that are connected to lab stands and a clear lucite cylindrical cover fitted into a circular groove notched into the base plate. A spring-loaded metallic sample stand is used to provide vertical pressures up to 150 psi against the rotating abrasive disk. Abrasive cloth attached to the disk is used to produce mechanical damage during operation. Since alignment of the rotating disk with respect to the sample is extremely critical for uniform damage production at the back-surface, the support fixture for the drive shaft connecting the motor and rotating disk was designed so that critical vertical and horizontal adjustments could be made before any experimental run. Rotary motion of the disk is provided by an external motor connected to the vertical head by a flexible drive shaft. Angular velocity is controlled by varying the input to the motor with a maximum rotation rate of 25,000 rpm recorded in the free running state, and 22,000 rpm in a typical run mode. In all cases, it was necessary to determine the rotation rate as a function of vertical pressure of the sample against the rotating disk. Total exposure time is monitored and control provided manually or automatically for pre-set time intervals.

Samples are mounted on the smooth face of the sample stand and the force adjusted by altering the compression of the spring attached to the stand. During operation of the unit, it was found that the flow rate of deionized water must be controlled carefully to provide proper cooling of the sample and removal of mass during abrasion. Total exposure or operational time was also extremely critical for GaAs wafers, although relatively less so for damage introduction in Si. In each case, the time of exposure was monitored and controlled manually or with an automatic "on-off" electronic timer.

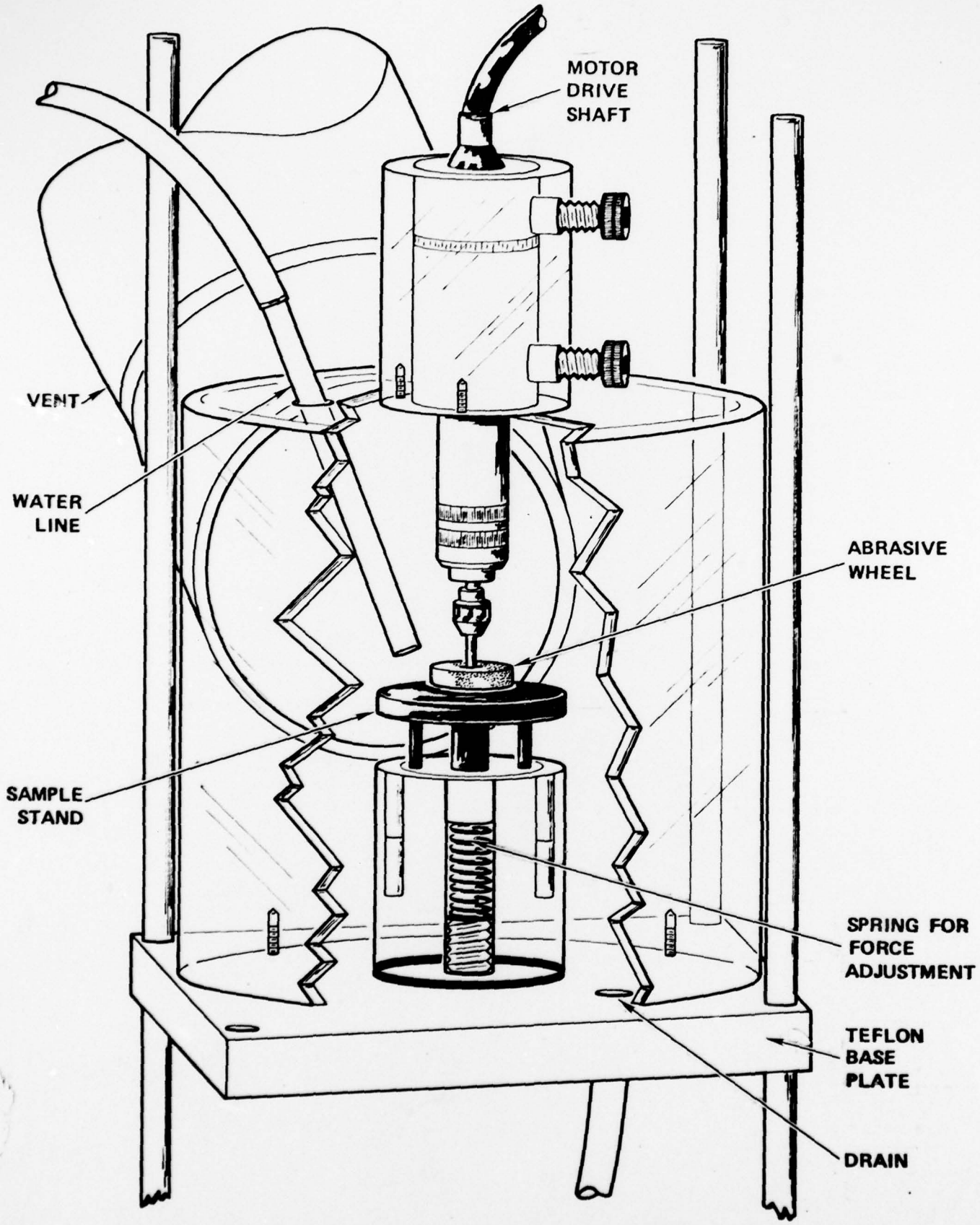


FIGURE 1. EXPERIMENTAL APPARATUS FOR CREATING BACK-SURFACE MECHANICAL DAMAGE

3. DAMAGE DISTRIBUTION AND STABILITY

3.1 MICROSTRUCTURAL DAMAGE

Gallium arsenide wafers used in these experiments were obtained from Crystal Specialties, Inc., Monsanto, and Laser Diodes. The samples were of (100) orientation ($\pm$ 1°) and doped with Cr or Si to levels of 0.008 and 10^8 Ω cm, respectively. Specimens were prepared for back-surface-damage experiments in the form of parallelopipeds or 5 mm x 5 mm lateral dimensions with a thickness of approximately 15 - 20 mils.

TRI-M-ITE (3M Corp.) paper disks containing silicon carbide particles of sizes 0.3 μm, 12.5 μm, 30 μm, and 60 μm, were used in these experiments. Rotation rates were varied between 1000 to 10,000 rpm and the sample exposure time was systematically altered in the range, 30 sec to 180 sec. A stationary platform pressure of 47 psi was experimentally found to yield the most adequate and reproduceable results.

Samples for transmission electron microscopy/diffraction (TEM/TED) analysis were prepared by conventional jet thinning from 2.5 mm x 2.5 mm specimens. To establish control data for each of the experiments, the microstructure of samples cut from as-received wafers was analyzed at both the front and back sides of polished specimens.

Figure 2 shows a representative series of bright-field electron micrographs obtained from GaAs wafers damaged at the back surface using a 30 μm abrasive particle size, 8,000 rpm rotation rate and exposure times between 30 sec and 3 min. At a 30 sec exposure time, edge dislocations lying in the (100) plane and inclined dislocation lines form continuous forested nests extending beneath the surface. After 1 min and 3 min of exposure, the dislocation density increases significantly and extremely complex forested regions are formed. The abrasive process produces a region of mass removal and circular grooves extending into the substrate at the back surface.

After 30 sec of exposure ≃ 0.7 mil of back-surface material is removed and grooves extending to a depth of ≃ 1.2 mils are observed in the scanning electron microscope. Similar groove depths are detected after 1 min and 3 min of exposure, but the mass removal thickness increases to ≃ 2.0 mils and

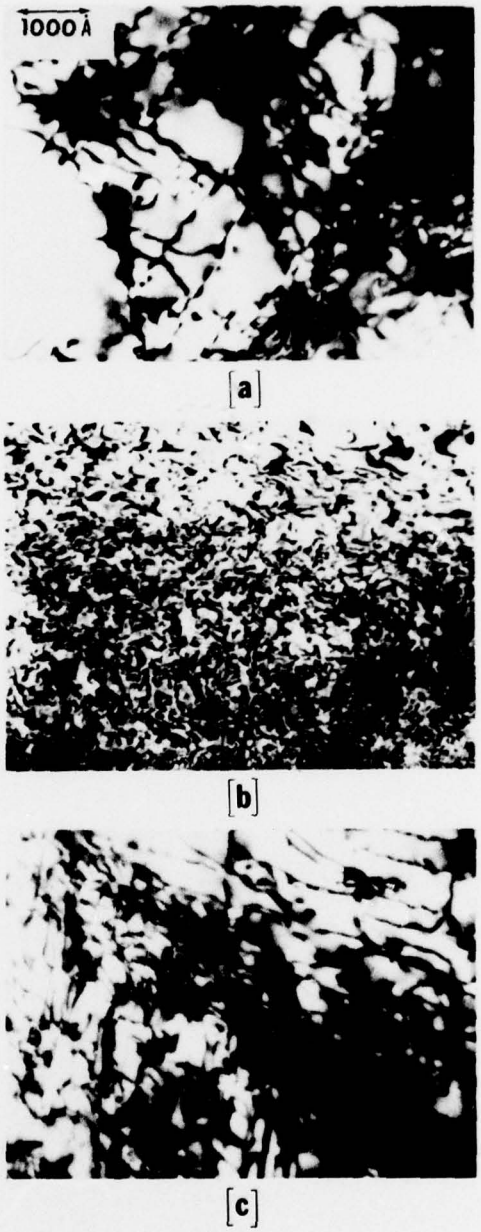


FIGURE 2. BRIGHT FIELD TRANSMISSION ELECTRON MICROGRAPHS OF BACK-SURFACE-DAMAGED GaAs WAFERS (PARTICLE SIZE= 30 μm, 8000 rpm). a) 30 sec exposure time; b) 1 min exposure time; c) 3 min exposure time

5 mils, respectively. Experiments conducted at similar exposure times using particle sizes of 0.3 μm, 12.5 μm and 60 μm show that the amount of mass removed increases significantly after 3 min of exposure and groove heights are approximately equal to the particle size.

In contrast to results obtained on Si, where broader, more complex grooving occurs as a function of exposure time, the distribution of grooving is relatively independent of exposure time. However, the mass removal rate is greatly increased for GaAs, and short exposure times are desirable. The results of experiments conducted under similar conditions with the rotation rate varied between 2000 and 8000 rpm suggested that the most uniform distribution of macroscopic damage was obtained at 8000 rpm.

In sharp contrast to earlier studies and to practices currently used by manufacturers in back-surface damage of Si wafers, we found that assessments of the concentration of microscopic damage introduced into the GaAs substrate cannot be characterized by the depth or distribution of macroscopic grooves and/or pits produced at the back surface. TEM analysis must be used routinely in these applications to identify the distribution of microstructural defects. In Figures 3 through 6, transmission electron micrographs show the distribution of damage at various depths for samples subjected to rotary abrasion at 8000 rpm for 30 sec at a vertical stage pressure of 47 psi, using particle sizes of 0.3 μm, 12.5 μm, 30 μm and 60 μm, respectively. In all cases, we observe a distribution of microstructural damage extending beneath the region of mass removal and macroscopic grooving. Hence, the experimental conditions used produce a laterally continuous sheet of dislocation lines in forested arrays and tangles that extend to a maximum observable depth of 1.5 μm below the depth of grooves at the back surfaces. In Figures 3 - 6, we observe that the maximum near-surface concentration is produced for the larger particle sizes. In addition, the density of dislocation lines decreases rapidly as a function of depth for the smaller particle sizes. In all samples examined, we detected no dislocation line structure at depths exceeding 1.5 μm.

In Figure 7, we show a plot of the dislocation line length density $\rho(cm/cm^3)$ at various depths from the back surface for the variable particle sizes used. For a particle size of 0.3 μm, the dislocation line density

FIGURE 3. BRIGHT FIELD TRANSMISSION ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (0.3 μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 7000 Å; c) d = 1.4 μm.

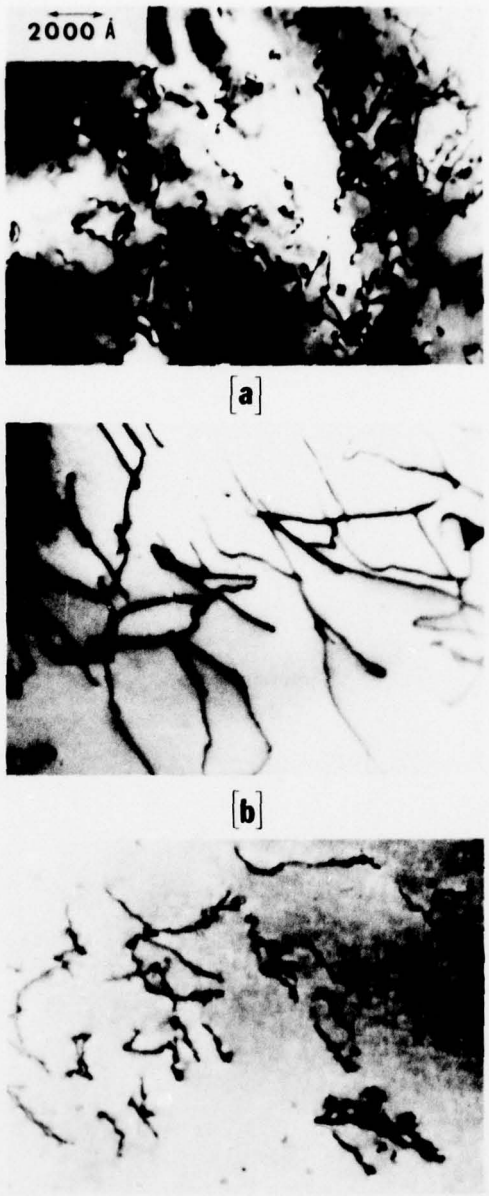


FIGURE 4. BRIGHT FIELD TRANSMISSION ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (12.5 μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 6000 Å; c) d = 1 μm.

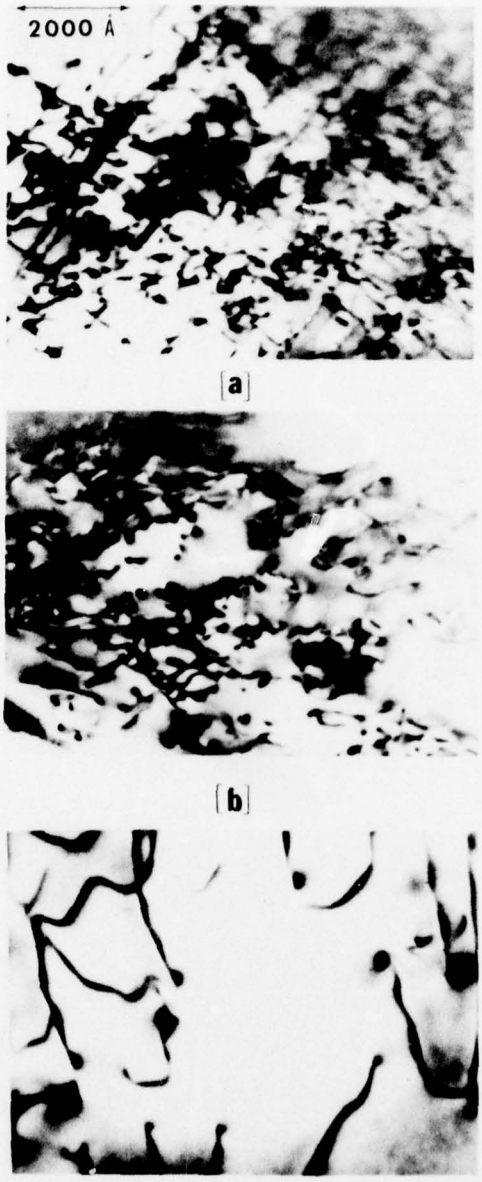


FIGURE 5. BRIGHT FIELD TRANSMISSION ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (30 μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 4000 Å; c) d = 1 μm.

[a]

[b]

[c]

FIGURE 6. BRIGHT FIELD ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (60 μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 7500 Å; c) d = 10.2 μm.

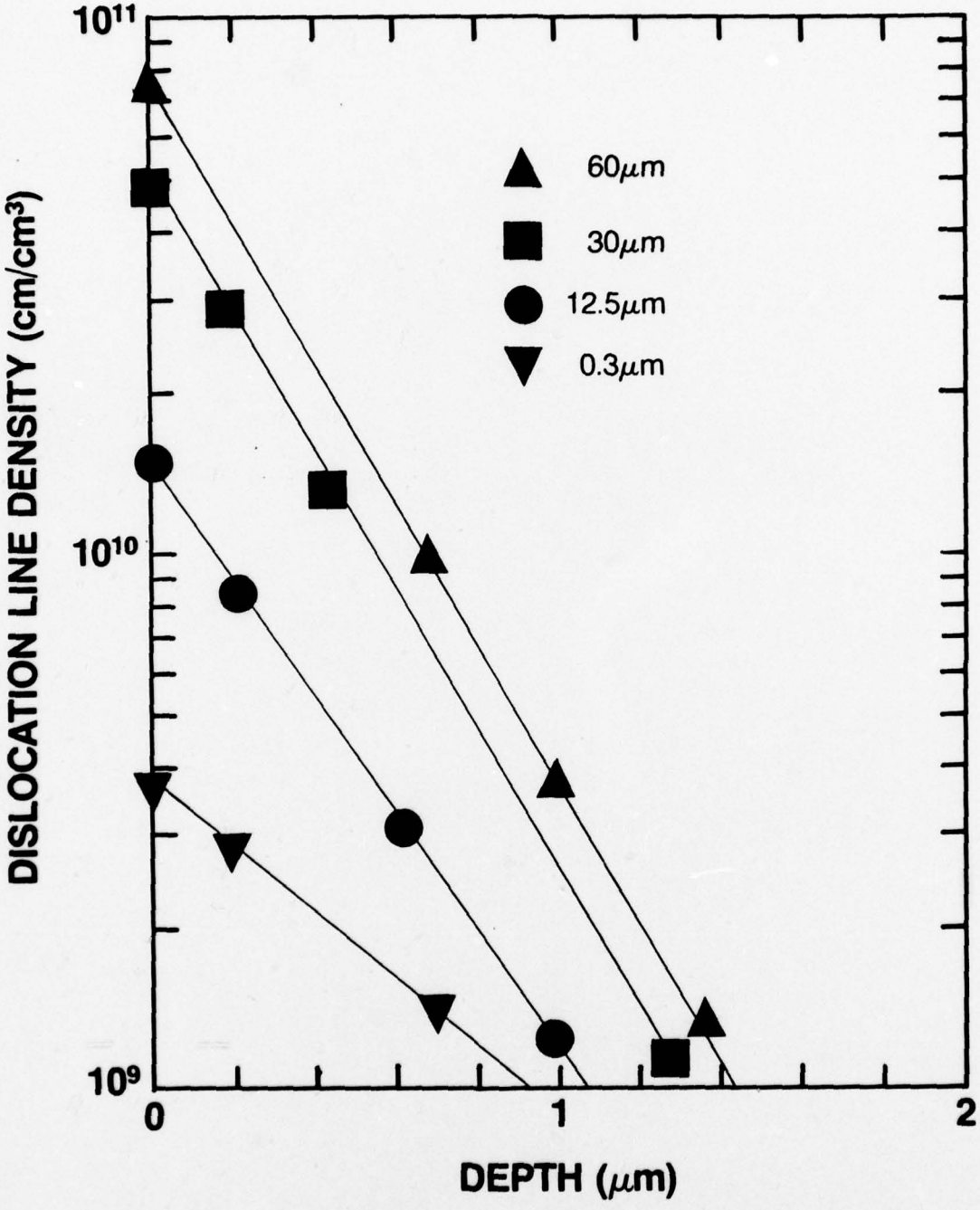


FIGURE 7. DISLOCATION LINE DENSITY VS DEPTH FOR VARIOUS PARTICLE SIZES (8000 rpm, 30 sec).

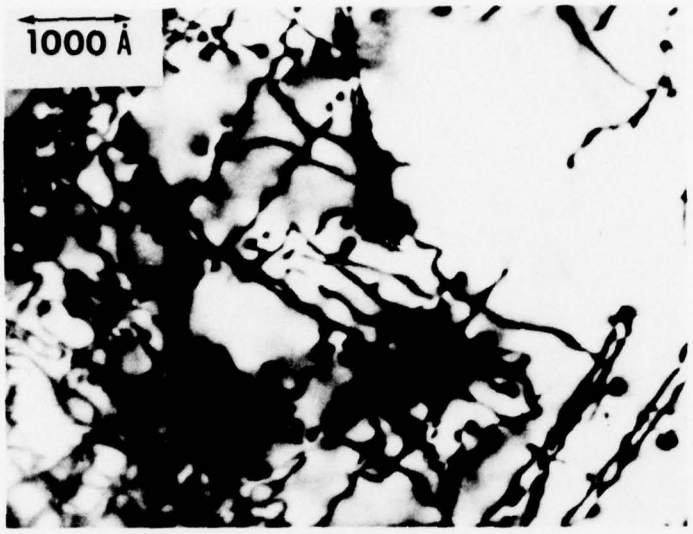
decreases from 3.7×10^9 cm/cm^3 in the near-surface region to negligibly small concentrations at depths $\lesssim 1.5$ μm. As the particle size is increased, the dislocation density also increased to a maximum of 7.2×10^{10} cm/cm^3 (particle size = 60 μm). In each case, we observe a negligible line density at depths $\simeq 1.5$ μm. Of particular interest, however, is the presence of a graded dislocation density observed reproducibly for samples used in these experiments. The slope of the concentration vs. depth line increases rapidly as a function of particle size, approaching saturation for particle sizes $\simeq 30$ μm.

The data show that the rotary back-surface damage technique produces a graded defect layer rather than a uniform layer of constant defect concentration. This result is of significance to the back-surface-gettering procedure since the resulting strain field at the back surface will also be sharply graded and defect and impurity gettering will be subsequently influenced, as discussed in the next sections.

3.2 THERMAL STABILITY

To evaluate the applicability of the gettering technique to a device processing line, it is necessary to define a stability time or period in which the defects will be retained at temperatures approaching those normally encountered in routine device fabrication or processing procedures. Therefore, we conducted a series of experiments in which back-surface-damaged wafers were coated on the front surfaces with a low-oxygen-content, plasma-deposited Si_3N_4 layer formed at 300° C and annealed at 800° C for periods in the range, ½ hr. to 6 hrs. After annealing, the nitride layers were removed and the samples prepared for TEM analysis by jet thinning from the front surface. Figure 8 shows a representative transmission electron micrograph obtained at the back surface of samples before and after annealing at 800° C for variable periods. As anticipated, we note a reduction in dislocation density as a function of annealing duration. In Figure 9, we show a plot of the unannealed fraction of dislocation lines

$$\left(\frac{\sum_{i=1}^{n} \rho i(x)}{\sum_{i=1}^{n} \rho o(x)} \right)$$



[a]

[b]

FIGURE 8. BRIGHT FIELD ELECTRON MICROGRAPHS OF BACK-SURFACE-DAMAGED WAFERS (30 μm PARTICLE SIZE, 8000 rpm, 30 sec) AFTER ANNEALING; a) 30 min; b) 180 min.

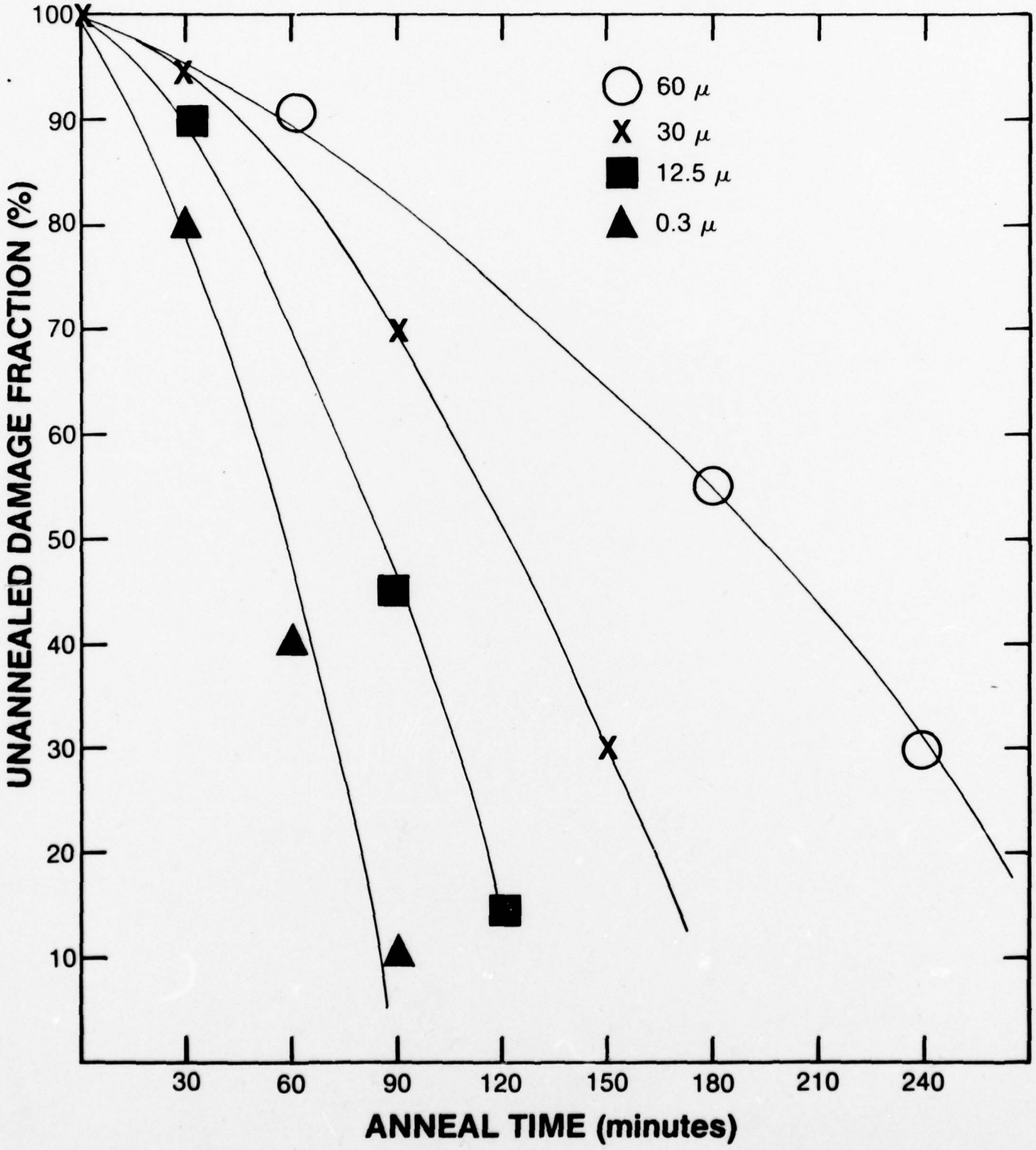


FIGURE 9. UNANNEALED FRACTION OF DAMAGE REMAINING AS A FUNCTION OF ANNEALING TIME.

as a function of annealing time at 800° C.

The increased dislocation density and complex forests produced by the larger particle sizes will require longer annealing times, whereas for the smaller particle sizes, annealing will occur more rapidly. In all cases, residual dislocation structures will remain in the samples after extended anneals at 800° C. However, for σ = 60 μm, unannealed damage factions < 10 to 15% gettering by dislocations will be ineffective. Similarly, residual structure remaining in samples damaged by smaller particles will not be efficient for impurity and defect gettering. Hence, a maximum stability time for gettering by dislocation lines at the back surface, is between 4 and 5 hrs. If the annealing time exceeds the damage stability time, then"reverse" annealing or "reverse" impurity gettering will likely occur, as has been noted in Si. This phenomenum is presently being explored in more detail for GaAs.

4. EFFECTS OF ENCAPSULATION LAYER

Since dielectric layers are routinely used as annealing caps for gettering or ion-implantation studies, it is essential that the encapsulation layers be examined to determine possible gettering or deleterious effects caused by the encapsulant during annealing. In previous studies by the author[9-12] and others,[13,14] it was shown that the presence of oxygen in silicon nitride encapsulating layers is associated with the outdiffusion of Ga and As from the GaAs substrates during annealing.

Alterations at the surface of a GaAs substrate annealed with nitride caps containing oxygen are also noted in the form of brown discoloration zones or layers relatively inert to chemical etching. Bozler, et al,[8] in studies of SiO_2/Si_3N_4 capped ion-implanted (back surface) GaAs samples, reported the presence of an inert surface layer after annealing and a slight or apparent cap-gettering effect on control (undamaged) wafers. In this investigation, we were concerned about possible gettering effects by the encapsulant and whether the currently used plasma deposited caps would be adequate for gettering studies. Silicon nitride caps used in this study were formed by low-temperature (300^{o} C) plasma deposition on GaAs at Avantek, Inc. Auger electron spectroscopy (AES) combined with in situ Ar-ion milling was used to obtain the chemical/depth profiles of the Si_3N_4 (GaAs) structures. The AES data were obtained by irradiating the sample with a 3 kV, 10 A electron beam and monitoring the differential spectrum of secondary electrons with a cylindrical mirrow analyzer during Ar-ion sputtering at a vacuum level of 5×10^{-5} Torr. A standard semiquantitative formalism[15] was used to analyze the AES data.

In Figures 10 and 11, we show representative chemical depth profiles (normalized) obtained on Si_3N_4/GaAs structures before annealing and after a 30-minute anneal at 800^{o} C in a flowing H_2 atmosphere. The unannealed sample shows a residual oxygen present throughout the film with no initial Ga or As outdiffusion from the substrate. After annealing, the second sample clearly shows that Ga and As have outdiffused from the substrate through the encapsulant to accumulate on the surface of the nitride film. This result is in agreement with recent results that show oxygen content in the nitride can

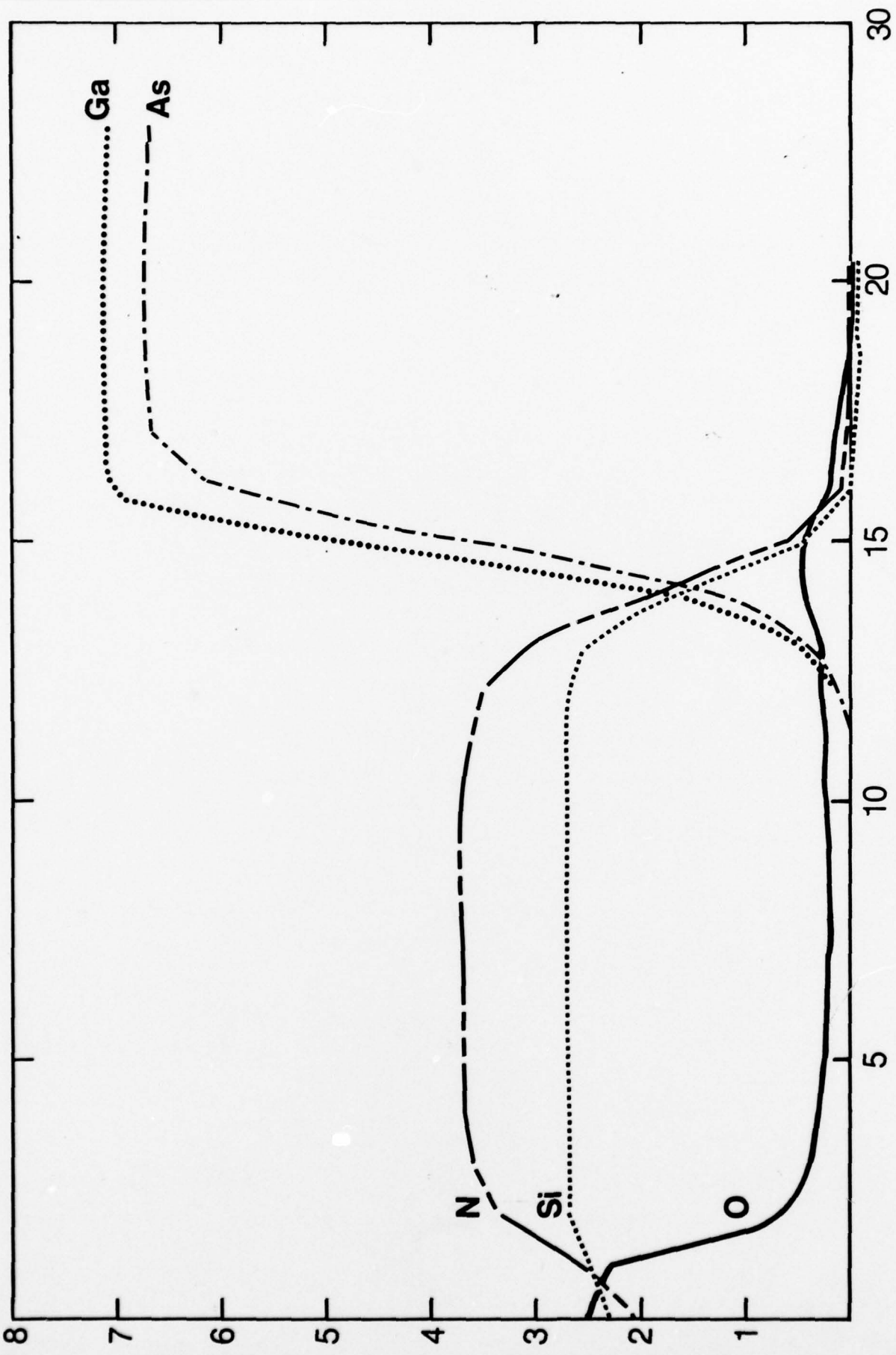


FIGURE 10. AES CHEMICAL DEPTH PROFILE (NORMALIZED) OF AS-DEPOSITED Si_3N_4 FILM ON GaAs.

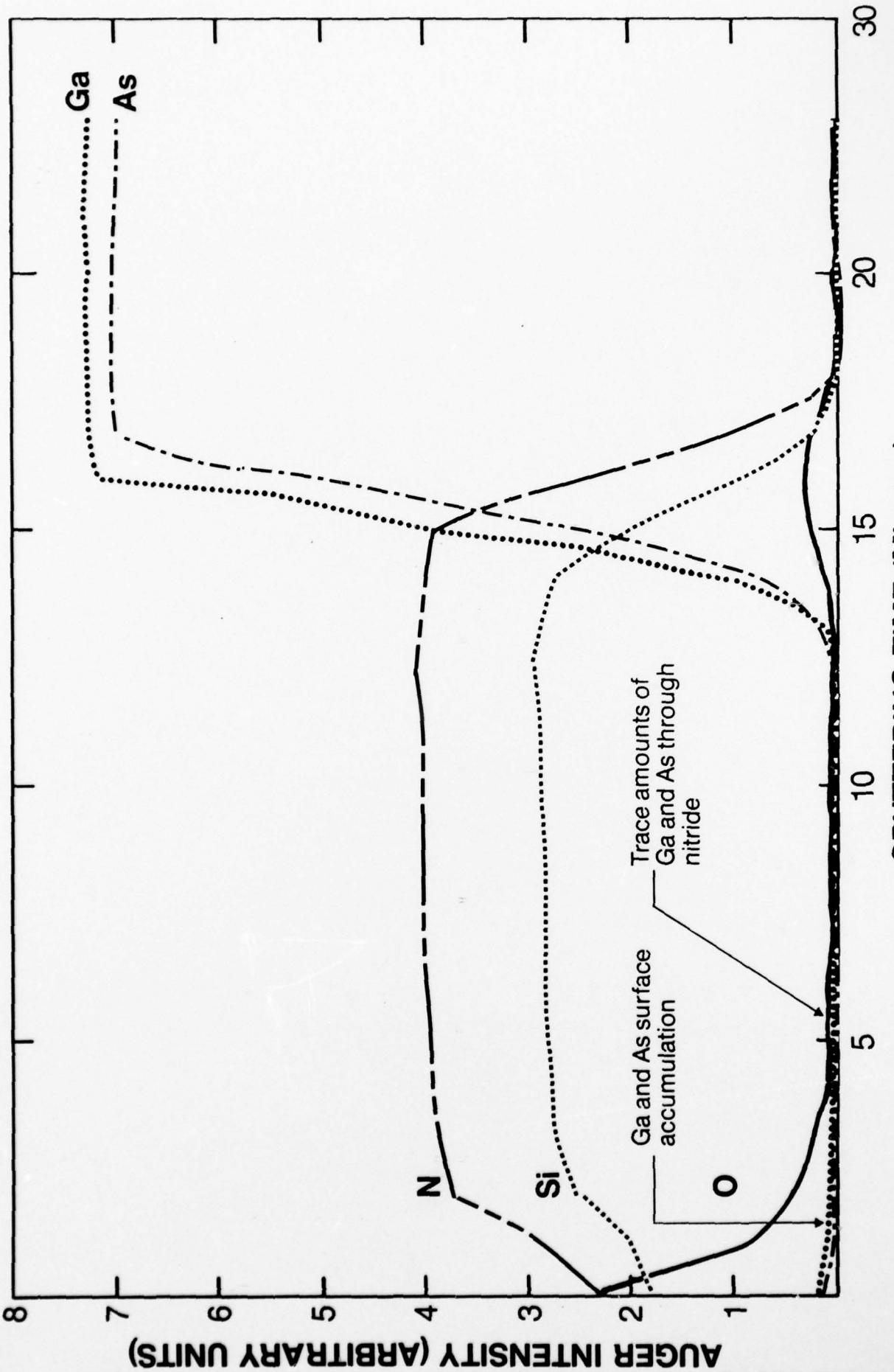


FIGURE 11. AES CHEMICAL DEPTH PROFILE (NORMALIZED) OF Si_3N_4 FILM ON GaAs.

be correlated with outdiffusion of Ga and As.

In separate experiments, we removed the caps of control and annealed structures by immersing them in a dilute HF solution. Examination in an optical microscope and scanning electron microscope (SEM) showed no apparent modification, discoloration or pitting at the surface.

To provide further comparison, we did AES profiling on Si_3N_4 caps known to contain a high concentration of oxygen. In Figure 12, we show the normalized AES profile of the annealed (850° C) Si_3N_4/GaAs structure. It is apparent that Ga has outdiffused through the cap to the surface of the film. However, in comparison to the results shown in Figures 10 and 11, the oxygen concentration is higher and the amount of Ga outdiffusion greater. After annealing, the same cap was removed in a separate experiment and examined optically and in an SEM. In both cases, a slightly discolored or nonuniform surface was observed with small regions showing resistance to conventional chemical etching.

We next prepared two sets of samples from the Si_3N_4 capped wafer provided by Avantek. In the first set of samples, the nitride layers were removed from the substrate by immersing the structure in a dilute HF solution. The remaining samples were first annealed at 800° C for 30 min in H_2 and the cap subsequently removed in HF. All samples were then immersed in a standard H_2SO_4: H_2O_2: H_2O (3:1:1) solution to expose defects or etch features on the (100) surface. Figure 13 shows representative optical micrographs of control and annealed sample surfaces after etching. Comparing Figure 13a) (control) and Figure 13b) (capped, annealed), we observe a slight reduction in the surface defect density, indicating a small apparent reduction in surface defect concentration. We then repeated the experiments on several sets of samples with essentially identical results, thereby supporting the contention that the encapsulant may exercise a small, but perceptible, defect gettering effect.

From the data obtained, we conclude that the quality of encapsulting layers can exercise some influence on defect gettering at the front surface. It is also apparent that outdiffusion of Ga and As should be suppressed, particularly for long annealing periods. In the present experiments, the oxygen concentration in nitride films can be correlated with Ga and As outdiffusion

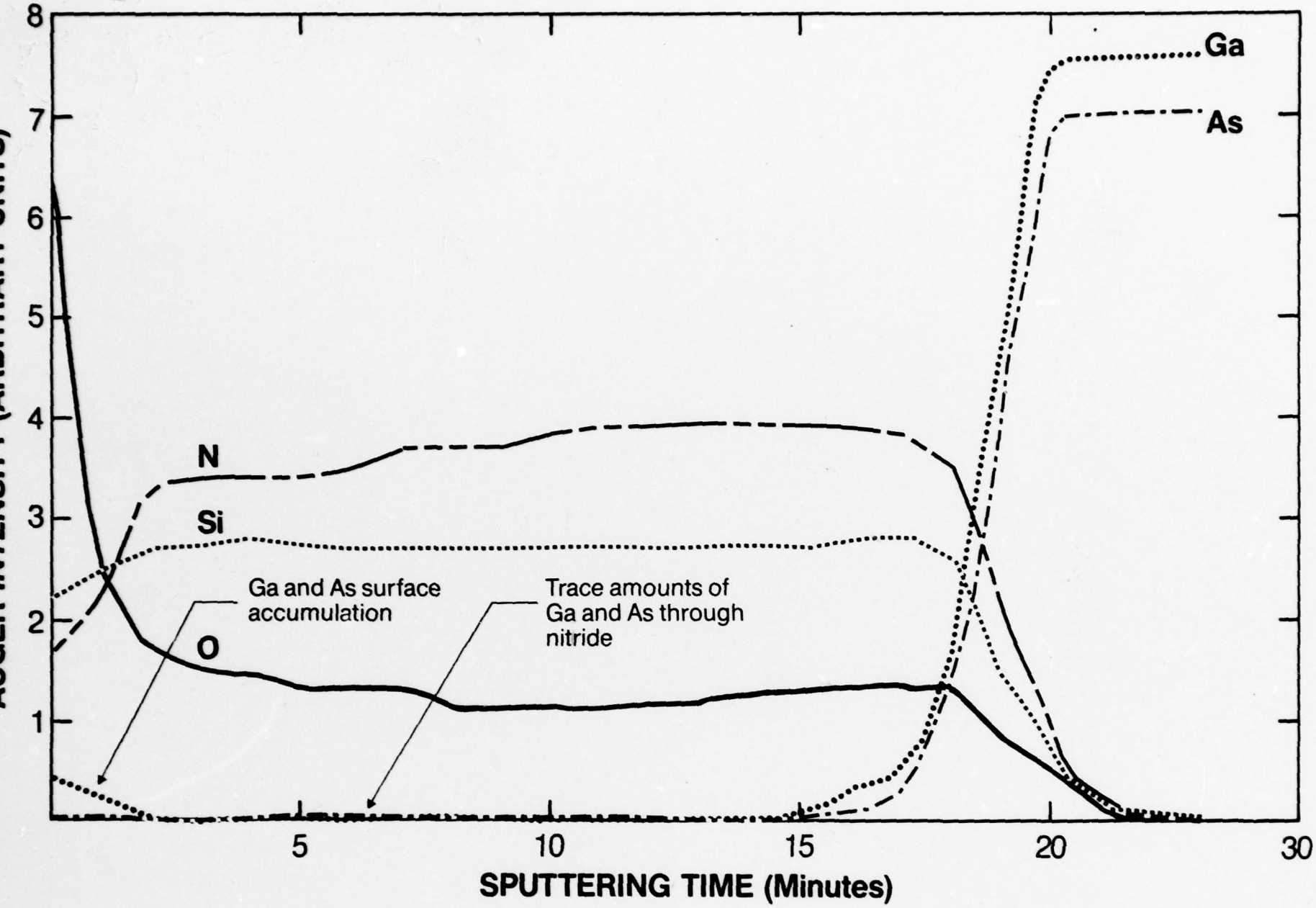
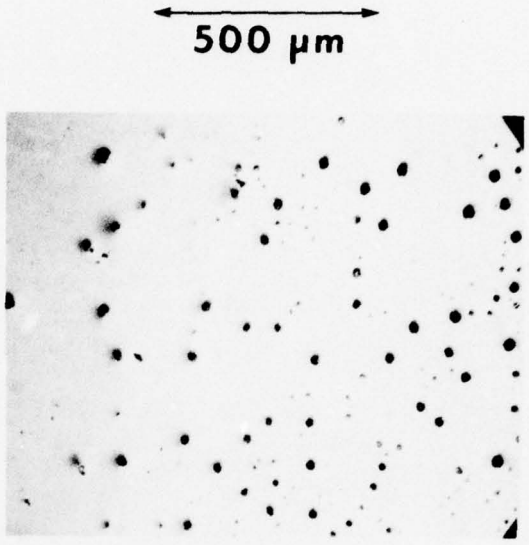
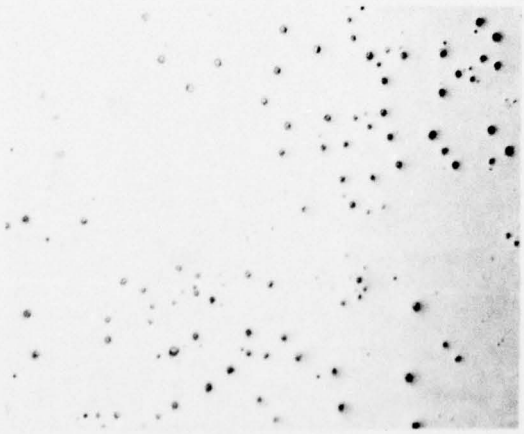


FIGURE 12. AES CHEMICAL DEPTH PROFILE (NORMALIZED) OF HIGH OXYGEN CONTENT Si_3N_4 FILMS ON GaAs AFTER ANNEALING (30 min, 850° C).



(a)



(b)

FIGURE 13. OPTICAL MICROGRAPHS SHOWING DEFECTS AT THE SURFACES OF CONTROL (UNANNEALED) AND ANNEALED Si_3N_4 CAPPED SAMPLES; a) Control; b) Annealed.

and the creation of vacancies in the rear surface region. The small gettering effect observed can then be associated with the presence of excess Ga and As vacancies at the surface or differential strain within the interfacial region.

5. DEFECT GETTERING

To evaluate the gettering efficiency of back-surface-damage wafers, we examined 50 samples prepared under a variety of experimental conditions. Since the required annealing cap was shown reproducibly to exert only a negligible effect on gettering of defects at the front surface, we assumed that all observable reductions could be primarily associated with strain introduced by defects at the oppoisite surface. In Figures 14 and 15, we show representative optical micrographs obtained at the front surfaces of control and back-surface damaged, annealed GaAs samples with (100) orientation, exposed to a pH controlled H_2SO_4:H_2O_2:H_2O (3:1:1) etch solution.

In Figure 14a), the control samples were coated with a 1000 Å plasma-deposited Si_3N_4 layer. After stripping the nitride layer in an HF solution, the samples were exposed to the (3:1:1) etch solution. Similarly, the sample in Figure 14b) was capped with Si_3N_4, and subjected to 30 seconds of mechanical damage using a 30 μm particle size and an 8000 rpm rotation rate. Subsequently, the sample was annealed at 800° C in flowing H_2 for 30 minutes and the cap removed in HF. After rinsing in DI water and drying, the sample was exposed to the (3:1:1) solution to reveal defect etch figures at the surface. The optical micrograph of the control sample shows an etch figure count of $\simeq 10^4/cm^2$, whereas after mechanical damaging the back surface and annealing, an etch figure density of $\simeq 90/cm^2$ is observed, representing a gettering efficiency of $\simeq$ 99.1%. In identical experiments on separate sets of samples, we obtained comparable efficiencies in the range, 92% to 97%.

In Figure 15, control and mechanically damaged samples were treated in a similar fashion, except that the particle size was reduced to 0.3 μm. The etch figure density in the control sample (Figure 15a)) is $\simeq 7 \times 10^3/cm^2$, whereas the etch figure concentration in the back-surface-damaged sample that was annealed is $\simeq 1.2 \times 10^3$, corresponding to a defect gettering efficiency of $\simeq$ 83%. Subsequent experiments showed good repeatability, with an average gettering efficiency of $\simeq$ 81%.

In all cases, we were able to demonstrate that the mechanical damage introduced in the back surface yields a significant improvement in substrate quality and reductions in defect concentration at the front surface of the wafer. Correlated TEM examination of samples exhibiting dislocation densities

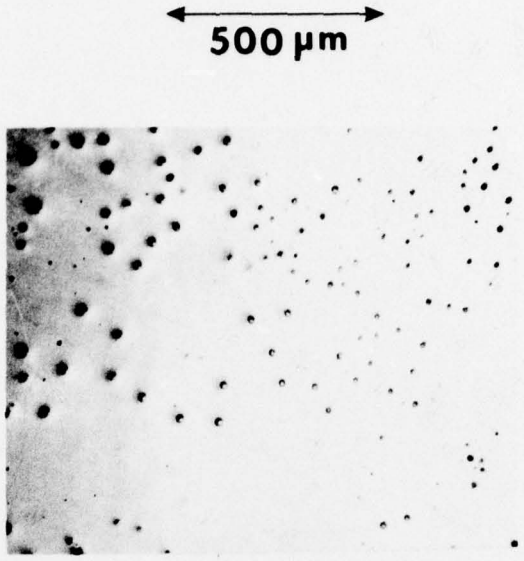
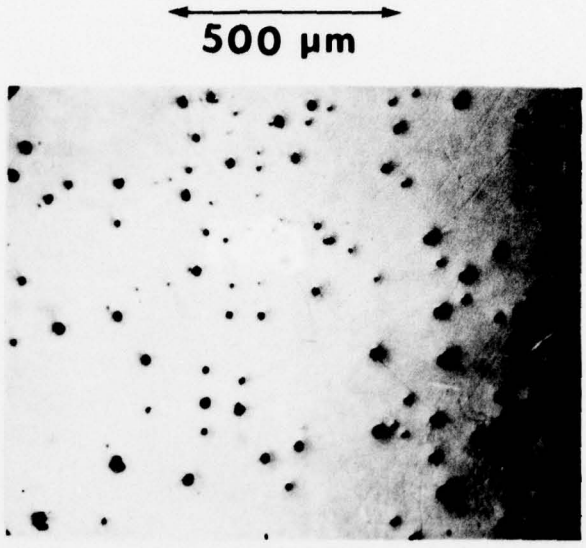


FIGURE 14. OPTICAL MICROGRAPHS OF FRONT SURFACES OF CONTROL AND BACK-SURFACE-DAMAGE GETTERED WAFER (30 µm PARTICLE SIZE, 8000 rpm, 30 sec); a) Control; b) Annealed, gettered.



(a)

(b)

FIGURE 15. OPTICAL MICROGRAPHS OF FRONT SURFACES OF CONTROL AND BACK-SURFACE-DAMAGE GETTERED WAFER (0.3 µm PARTICLE SIZE, 8000 rpm, 30 sec); a) Control; b) Annealed, gettered.

(etch pit counts) $\geq 10^4/cm^2$ showed similar reductions in defect density after damaging and annealing. However, in several cases, localized regions of high dislocation density were observed on control samples. Examinations of gettered samples obtained from the same wafer showed no apparent dislocation nests and a significant recuction in the number of dislocations intersecting the (100) surface.

In a correlated set of experiments, we implanted the back surfaces of 10 GaAs samples with 350 keV Ne ions to a dose of 10^{16} ions/cm^2. All implants were done at room temperature and the front surfaces capped with 1000 Å thick Si_3N_4 layers. After annealing at 800° C for 30 min, the encapsulation layer was stripped and exposed to the surface etch. A defect density of $\simeq 6.6 \times 10^3/cm^2$ was observed on the unannealed control sample in Figure 16a). After annealing, the defect density at the front surface of the implanted sample decreased to $\simeq 1.7 \times 10^3/cm^2$ (Figure 16b), with an apparent gettering efficiency of 74%. In all samples examined, we were unable to obtain gettering efficiencies comparable to values routinely observed for the mechanically damaged samples. It is apparent that damage stability during thermal annealing is an important factor in defect gettering. To increase the effectiveness of ion-implantation gettering, it will be necessary to either increase the damage retention time or provide a graded damage profile by multiple implants of varying dose and energy. Additional experiments are currently in progress to improve ion-implantation defect gettering in GaAs.

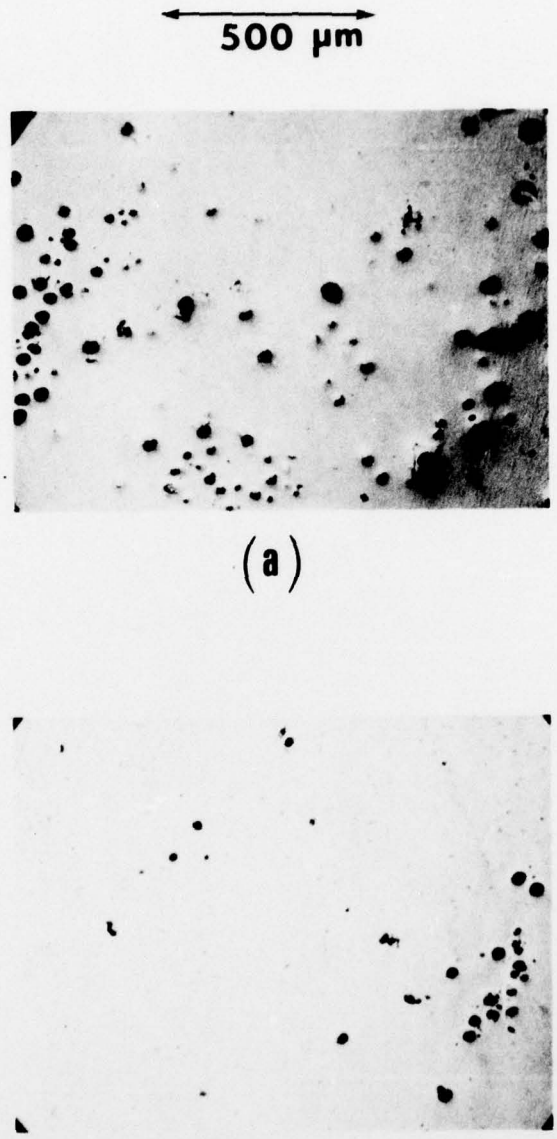


FIGURE 16. OPTICAL MICROGRAPHS OF FRONT SURFACES OF CONTROL AND ION IMPLANTATION GETTERED WAFER; a) Control; b) Implanted (back surface), 350 keV Ne, $10^{16}/cm^2$, annealed 800° C, 30 min).

6. GOLD AND CHROMIUM IMPURITY GETTERING

Although a number of studies have shown that heavy metals and other impurities can be effectively gettered in Si by ion-implantation or mechanical damage, there have been no extensive investigations on the gettering of Au and Cr by defects in GaAs. The purpose of these experiments was to determine if impurities can be gettered by defects introduced by mechanical damage at the back surface of GaAs wafers.

Silicon- and chromium-doped wafers of (100) orientation were obtained from Monsanto, Inc. and Crystal Specialties, Inc. Resistivities were of the order of 10^8 Ω-cm (Cr-doped) and ≃ .008 Ω-cm (Si-doped). After cleaning and degreasing the wafer surfaces, specimens were exposed to rotary mechanical abrasion using particle sizes of 0.3 μm, 12.5 μm, 30 μm, and 60 μm. Experimental techniques were identical to those described in the previous sections. For gettering experiments, we coated the polished front surfaces with gold or chrome powder (99.99% purity) suspended in methanol. Afterwards, the samples were weighed to assure uniform concentrations for each experiment. Control samples (no back-surface damage) were similarly coated for comparative analysis. All samples were then annealed at 800° C for 30 min to one hour in flowing H_2.

Secondary ion mass spectroscopy (SIMS) and Cs-ion milling[16] was used to obtain impurity concentration profiles at the back surface of each sample. A gold implanted sample was used to obtain both concentration and depth calibration for the annealed samples.

Figure 17 shows a plot of the log Au-ion intensity and concentration as a function of depth from the back surface for annealed samples damaged by rotary abrasion using particle sizes, σ, in the range, 0.3 μm to 60 μm. We observe that the maximum concentration of gettered Au atoms increases rapidly as a function of increasing particle size. For a particle size, 0.3 μm, the maximum Au concentration is located within a narrow near-surface region of width ≃ 500 Å. However, for $\sigma \geq 30$ μm, the Au is distributed throughout the dislocation line region. In comparative studies of a number of control samples (no back-surface damage) containing Au at the front surface and annealed under similar conditions, we observe no Au at the back surfaces.

FIGURE 17. SIMS PROFILES OF Au AT BACK SURFACES OF DAMAGED WAFERS.

To determine the correlation of Au concentration and dislocation line density, we compared the integrated impurity and dislocation densities in the ratio:

$$\alpha = \int_{o}^{d} \frac{C(x)\ dx}{\rho(x)} \quad ,$$

where $C(x)$ (cm^{-3}) is the concentration of Au as a function of depth, $\rho(x)$ (cm/cm^{-3}) is the measured dislocation line density in sectioned samples over the depth, d(cm) at the back surface ($\rho \neq o$). Calculations of α, then, provide a dimensionless number defining the number of impurity atoms associated with each dislocation line.

Figure 18 shows a plot of α vs particle size, using the previous equation and data from Figures 7 and 17. The graph illustrates a linear dependence of α and particle size. Since the dislocation density is proportional to the size of the abrasive particle, it can be inferred that the gettering efficiency is also proportional to the dislocation content at the back surface. When $\alpha = 1.5 \times 10^5$, there are approximately 10^5 Au atoms associated with each dislocation line at the back surface. For an average line length $\simeq 0.5$ μm, there are then $\simeq 10^3$ sites available along the core of a dislocation line for trapping of individual impurity atoms. However, since $\alpha = 1.5 \times 10^5$, the number of Au atoms present greatly exceeds the available core sites for trapping, and the Au is not trapped along core sites but is present either in the form of impurity clouds surrounding dislocation lines or precipitates pinned at the edges of dislocations.

To obtain additional information on the possible location of Au in relation to microstructure at the back surface, we prepared annealed samples for TEM/TED analysis. For comparison, we also examined damaged (control) samples prepared under identical conditions but annealed with Si_3N_4 rather than Au on the front surface and undamaged (control) samples coated with Au and annealed. Figure 19 shows an electron micrograph obtained on a back-surface-damaged sample (σ = 60 μm, 8000 rpm, 30 sec) containing Au at the front surface after annealing for 40 minutes in flowing H_2. The presence of precipitates can be noted along the length of these dislocation lines in the bright-field micrograph shown in Figure 19. Corresponding dark-field micrographs also

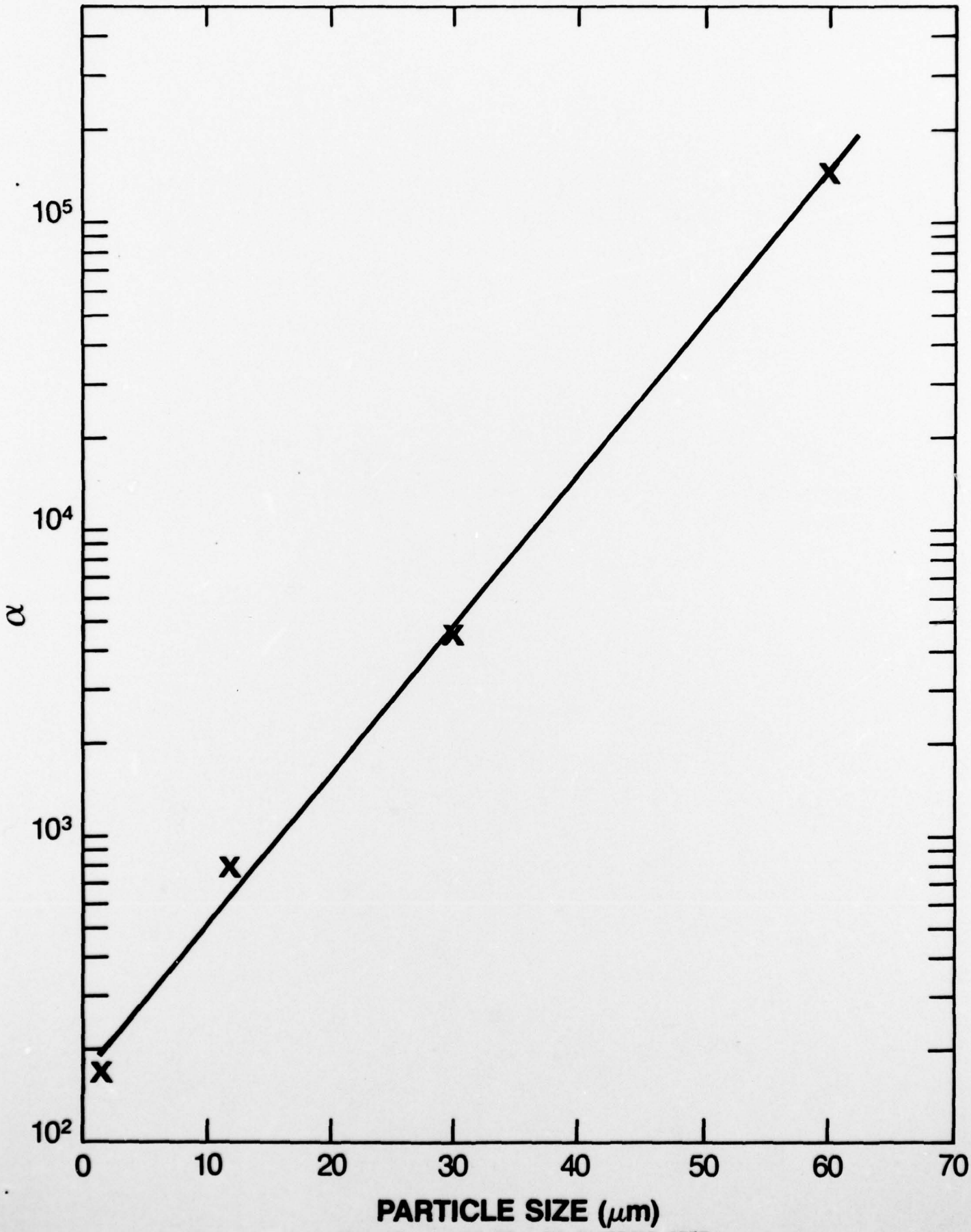


FIGURE 18. GRAPH OF α VS PARTICLE SIZE.

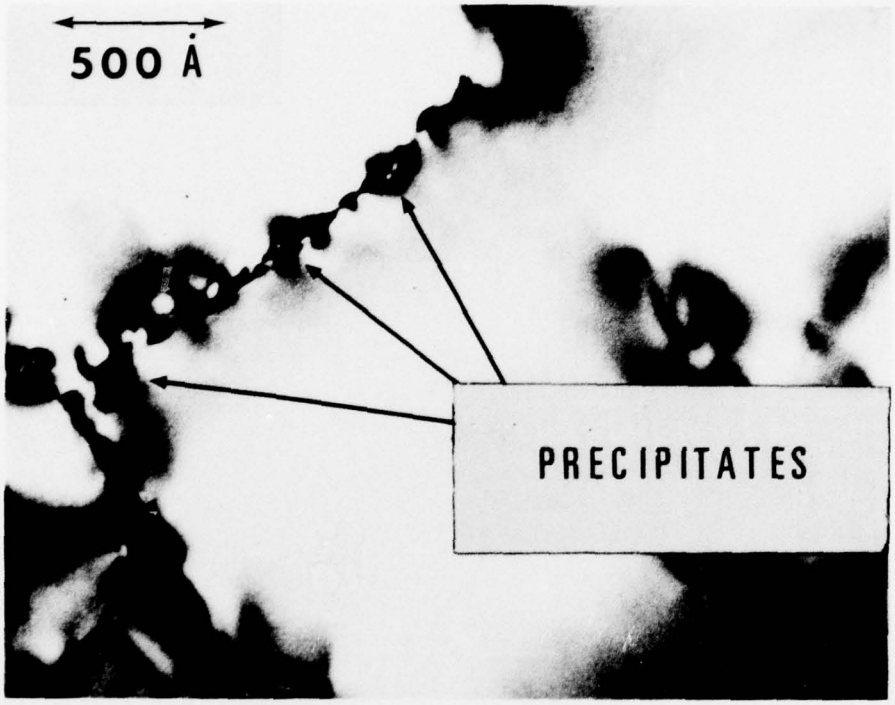


FIGURE 19. BRIGHT FIELD ELECTRON MICROGRAPH SHOWING PRESENCE OF Au PRECIPITATES ALONG DISLOCATION LINES.

confirm the presence of Au on dislocation lines. In all samples examined, we detected similar decoration of the dislocation line structure by precipitates. In contrast, we observe no evidence of precipitation along dislocation lines in any of the control samples prepared and annealed in the same manner. We can, therefore, conclude that Au is present in the form of precipitates pinned along dislocation lines.

If, indeed, the Au is predominantly localized along dislocation lines, it would be interesting to estimate the number of Au atoms pinned along each line using TEM data. From a number of micrographs, the mean (image) diameter of precipitates was found to be $\simeq$ 100 A. Assuming an actual diameter, $d_o \simeq 50$ Å, and $d_{Au} \simeq 2.74$ A, the number of Au atoms contained in each precipitate region is $\lesssim 6 \times 10^3$. The mean number of precipitates per dislocation line was then determined and the Au concentration calculated to be $\simeq 0.95 \times 10^5$ atoms/line. In contrast to the corresponding value of $\alpha = 1.5 \times 10^5$ atoms/line calculated from SIMS and TEM data (Figure 18), we find reasinably good agreement, particularly in terms of the experimental uncertainties in adequately imaging all of the precipitates selectively pinned along dislocation lines.

Similar experiments were conducted on back-surface-damaged samples containing a Cr layer on the front surface. After annealing for 40 min at 800° C in flowing H_2, we observe detectable concentrations of Cr within the region containing dislocations. In Figure 20, we show representative AES spectral data obtained from the back surface at a depth of $\simeq$ 1000 Å. Chromium is clearly present at levels of $\simeq$ 0.7 atomic percent. At depths of 1 μm, Cr is still present, decreasing to concentrations below the detection capability of AES for depths > 1.2 μm. Additional SIMS profiling is currently in progress to obtain quantitative data on the concentration of gettered Cr as a function of depth.

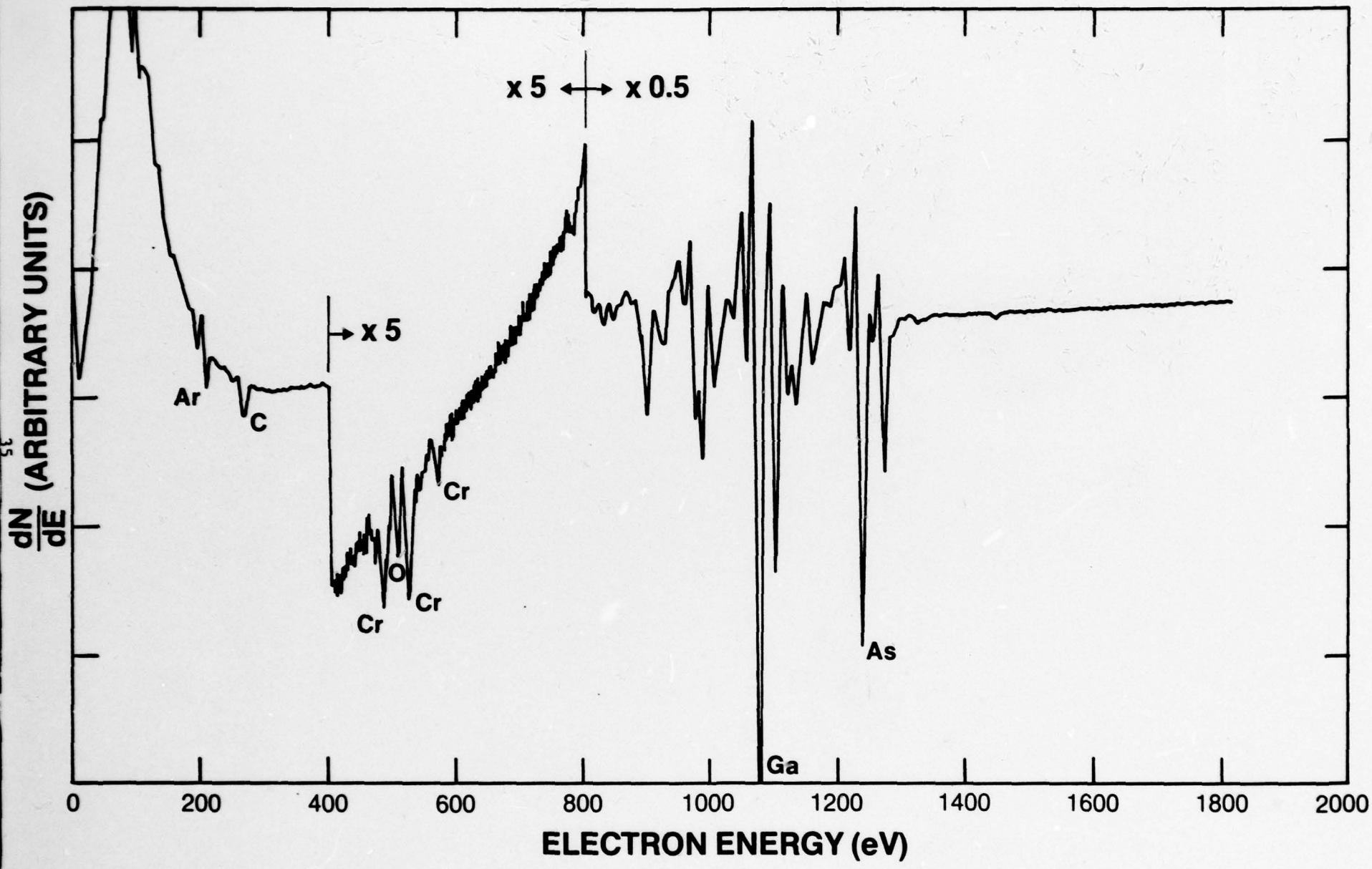


FIGURE 20. AES CHEMICAL DEPTH PROFILE OF BACK-SURFACE-DAMAGED WAFER AT DEPTH OF 1000 Å SHOWING THE PRESENCE OF Cr GETTERED BY DISLOCATIONS.

7. CONCLUSIONS AND FUTURE EXPERIMENTS

In the first six months, we have developed a prototype unit for introducing back-surface damage in Si and GaAs wafers and have demonstrated that the process can be optimized to produce adequate gettering of defects and impurities in GaAs. It has been shown for the first time that Cr and Au impurities can be gettered by back-surface mechanical damage. Dislocation density gradients and corresponding strain field gradients at the back surface are responsible for the gettering action observed.

Contrasting experiments performed on Ne-implanted GaAs samples have shown mechanical damage gettering to be superior and more cost effective. In both cases, the annealing cap was shown to exercise a small, but perceptible, influence on gettering of defects at the front surface. Cap gettering was shown to be attributable, in part, to the outdiffusion of Ga and/or As from the substrate, creating localized vacancy-rich regions that aid in defect annihilation. Improvements in capquality and the elimination of oxygen from nitride encapsulants should aid in reducing apparent cap gettering effects.

Of particular interest for both Si and GaAs gettering is the problem of thermal stability of defects during annealing; the stability period will define the usable time of active gettering during processing cycling or device fabrication. Beyond a fixed period (4 - 5 hours at 800° C for mechanically induced damage), reverse gettering will occur and impurities will be released from dislocations at the back surface to move into the bulk toward the front surface. For ion-implantation gettering, the problem is an especially acute one, since the induced damage is largely annealed after 1 hour.

To improve the stability time, we are continuing experiments using an As-doped SiO_2 cap on the back surface to prevent the loss of As vacancies. It is conceivable that dislocation structure and ion-induced damage can be retained for longer periods in the presence of excess As at the interface.

We are also beginning experiments on the growth of liquid phase epitaxial/vapor phase epitaxial (LPE/VPE) layers on back-surface-damaged substrates. Of particular concern in these experiments is both the stability time of damage and the reduction of Cr diffusion across the interface into the epitaxial layers. Recent studies[17] at Plessey Inc. have shown that Cr outdiffuses readily from

the substrate (non-gettered) producing a level of $\simeq 10^{15}/cm^3$ in the epi-layer. Our studies have demonstrated that Cr can be effectively gettered at the back surface when the distribution of damage is optimized. It is of importance, however, to determine if the observed outdiffusion across the epi-layer/substrate interface can be reduced or eliminated by strain fields introduced by damage at the back surface.

To further investigate the problem of impurity diffusion, we are ion-implanting Cr into the front surface and annealing prior to growth of the epitaxial layer on control and back-surface-damaged wafers. Using SIMS, TEM and Hall-effect profiling, we will be able to determine more about the influence of structure and impurities on epi-layer quality.

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